In the Claims:

Please amend claims 1, 3, 9, 15, 17 and 18. Please add new claims 21-26.

The claims are as follows:

1. (Currently Amended) An integrated circuit comprising:

a set of bitlines;

a set of data lines;

a coupling circuit that ~~couples~~ directly connects each respective data line to a first respective bitline or to a second respective bitline based on a steering signal, said second respective bitline being adjacent to said first respective bitline; and

a circuit that maintains said first respective bitline at a desired potential after said data line is coupled to said second bitline.

2. (Original) The integrated circuit of claim 1, wherein a number of said bitlines in said set of bitlines exceeds a number of data lines in said set of data lines.

3. (Currently Amended) The integrated circuit of claim 2, wherein each said data line is ~~coupled~~ connected to only one of said bitlines and each said data line is ~~coupled~~ connected to a different bitline.

4. (Original) The integrated circuit of claim 1, wherein said first respective bitline maintained at said desired potential is a failed bitline.

5. (Original) The integrated circuit of claim 1, wherein said desired potential is ground.

6. (Original) The integrated circuit of claim 1, wherein said data lines transfer data in parallel to said bitlines and said bitlines are coupled in parallel to one or more memory cells.

7. (Original) The integrated circuit of claim 1, wherein all said data lines in said set of data lines are arranged in a serial order and further including:

means for coupling each data line, after said data that has been coupled to said second respective bitline, to corresponding respective second bitlines.

8. (Original) The integrated circuit of claim 1, wherein said steering signal indicates which bitlines of said set of bitlines are failed bitlines.

9. (Currently Amended) A method of replacing, in an integrated circuit having a multiplicity of data lines and a multiplicity of bitlines, a first bitline with a second bitline comprising:

providing a set of said multiplicity of said bitlines;

providing a set of said multiplicity of said data lines;

~~coupling~~ connecting each respective data line to a first respective bitline or to a second respective bitline through a switch and based on a steering signal supplied to said switch, said second respective bitline being adjacent to said first respective bitline; and

maintaining said first respective bitline at a desired potential after said data line is coupled to said second bitline.

10. (Original) The method of claim 9, wherein a number of said bitlines in said set of bitlines exceeds a number of data lines in said set of data lines.

11. (Currently Amended) The method of claim 10, wherein each said data line is ~~coupled~~ connected to only one said bitlines and each said data line is ~~coupled~~ connected to a different bitline.

12. (Original) The method of claim 9, wherein said first respective bitline maintained at said desired potential is a failed bitline.

13. (Original) The method of claim 9, wherein said desired potential is ground.

14. (Original) The method of claim 9, wherein said data lines transfer data in parallel to said bitlines and said bitlines are coupled in parallel to one or more memory cells.

15. (Currently Amended) The method of 9 wherein all said data lines in said set of data lines are arranged in a serial order and further including:

~~coupling~~ connecting each data line, after said data that has been ~~coupled~~ connected to said second respective bitline, to corresponding respective second bitlines.

16. (Original) The method of claim 9, wherein said steering signal indicates which bitlines of said set of bitlines are failed bitlines.

17. (Currently Amended) A content addressable memory comprising:

a set of bitlines;

a set of data lines, a number of said data lines less than a number of said bitlines;

a set of read lines, a number of said read lines equal to said number of said data lines, each said read line coupled to one corresponding bitline of said set of bitlines;

means for ~~coupling~~ directly connecting each respective data line to a first-respective bitline or to a second respective bitline based on a steering signal, said second respective bitline being adjacent to said first respective bitline;

~~means for directing a first respective read line coupled to said first respective bitline to a second respective read line coupled to said second respective bitline in response to said steering signal~~ means for coupling each respective read line to a first respective read line or to a second respective read line based on said steering signal, said second respective read line being adjacent to said first respective read line; and

means for maintaining said first respective bitline at a known fixed state after said data line is ~~coupled~~ connected to said second respective bitline.

18. (Currently Amended) The content addressable memory of claim 17, wherein all said data lines in said set of data lines are arranged in a serial order and all said read lines in said set of read lines are arranged in a serial order and further including:

means for ~~coupling~~ directly connecting each respective data line, after said respective data line ~~that~~ has been ~~coupled~~ connected to said second respective bitline, to a corresponding third respective ~~second~~ bitline[[s]], said third respective bitline immediately adjacent to said second respective bitline; and

means for ~~switching~~ directly connecting each respective read line, after said respective read line ~~that is switched~~ has been connected to said ~~immediately adjacent~~ second respective read line, to a third respective ~~corresponding~~ ~~immediately adjacent~~ read line[[s]], said third respective read line immediately adjacent to said second respective read line.

19. (Original) The content addressable memory of claim 17, further including:

one or none bitlines between said first respective bitline and said second respective bitline; and

one or none read lines between said first respective read line and said second respective read line.

20. (Previously Presented) The content addressable memory of claim 17, wherein said steering signal indicates which bitlines of said set of bitlines are failed bitlines and is derived from fuse latches.

21. (New) The integrated circuit of claim 1, wherein said coupling circuit includes a latch stage connected to a switch stage.

22. (New) The integrated circuit of claim 1, further including an additional coupling circuit that disconnects each respective data line connected to a second respective bitline by said coupling circuit from said second respective bitline and directly connects each respective data line to a third respective bitline based on said steering signal, said third respective bitline adjacent to said

second respective bitline, said additional coupling circuit connected between said coupling circuit and said set of bitlines.

23. (New) The integrated circuit of claim 22, wherein said coupling circuit includes a first latch stage connected to a first switch stage and said additional coupling circuit includes a second latch stage connected to a second switch stage.

24. (New) The method circuit of claim 9, wherein said coupling circuit includes a latch stage connected to a switch stage.

25. (New) The method of claim 9, further including providing an additional coupling, said additional coupling circuit disconnecting each respective data line connected to a second respective bitline by said coupling circuit from said second respective bitline and directly connecting each respective data line to a third respective bitline based on said steering signal, said third respective bitline adjacent to said second respective bitline, said additional coupling circuit connected between said coupling circuit and said set of bitlines.

26. (New) The method of claim 25, wherein said coupling circuit includes a first latch stage connected to a first switch stage and said additional coupling circuit includes a second latch stage connected to a second switch stage